AMENDMENTS TO THE SPECIFICATION

Please amend paragraph **[0012]** as follows.

Figure 1D illustrates a CCFL circuit 100B, also described by Fujimura, for regulating the output voltage of PZT 108 by controlling the duty cycle. Note that similar reference numerals in the figures refer to similar components. In CCFL circuit 100B, resistors 111 and 112 are connected in series between node N3 and VSS, thereby forming a voltage divider. In this manner, a line 117 connected to node N5 between ~~transistors~~ resistors 111 and 112 can be used to detect the output voltage of PZT 108 at node N3. Once again, an error amplifier EA compares the rectified voltage to a set reference voltage. The amplified EA output signal controls a pulse width modulation (PWM) oscillation circuit. The output of the PWM oscillation circuit, in turn, controls the duty cycle of a driving waveform to a driver, which generates the non-overlapping clock signals to transistors 104 and 105. As the duty cycle of this driving waveform increases, which results in having p-type transistor 104 conduct longer and having n-type transistor 105 conduct less, the amplitude of the signal at node N3 increases. Thus, this control loop attempts to regulate the brightness of CCFL 110 by controlling the duty cycle of the driving waveform to the driver, thereby changing the amplitude of the sinusoidal waveform at node N3. In an alternative embodiment, resistors 111 and 112 can be connected to node N2 via line 116. Thus, this control loop also attempts to regulate the brightness of CCFL 110 by controlling the duty cycle of the driving waveform to the driver, this time by changing the sinusoidal waveform at node N2. In yet another alternative embodiment, Fujimura describes substituting a PWM oscillation circuit for the VCO of Figure 1A. Fujimura indicates that such an embodiment regulates

the current through CCFL 110 by controlling the duty cycle of the driving waveform to the driver.

6a contd.